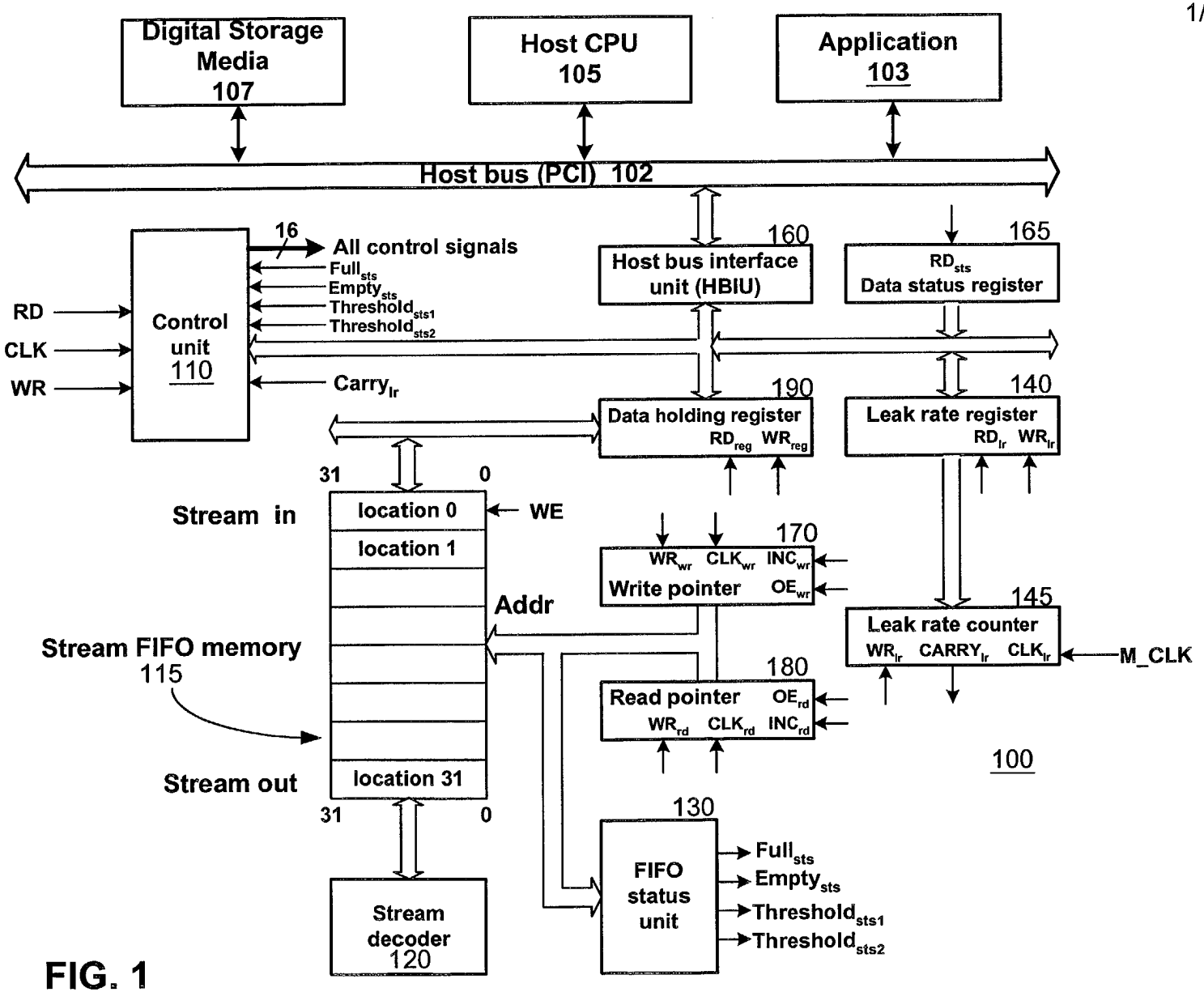
Digital Storage Media 107
Host CPU 105
Application 103
Host bus (PCI) 102
16
All control signals
Full_sts
Empty_sts
Threshold_sts1
Threshold_sts2
Carry_lr
RD
CLK
WR
Control unit 110
160
Host bus interface unit (HBIU)
165
RD_sts Data status register
190
Data holding register RD_reg WR_reg
140
Leak rate register RD_lr WR_lr
31
0
Stream in
location 0
location 1
location 31
WE
Addr
170
WR_wr CLK_wr INC_wr
Write pointer OE_wr
145
Leak rate counter WR_lr CARRY_lr CLK_lr
M_CLK
180
Read pointer OE_rd
WR_rd CLK_rd INC_rd
Stream FIFO memory 115
Stream out
100
130
FIFO status unit
Full_sts
Empty_sts
Threshold_sts1
Threshold_sts2
Stream decoder 120

FIG. 1

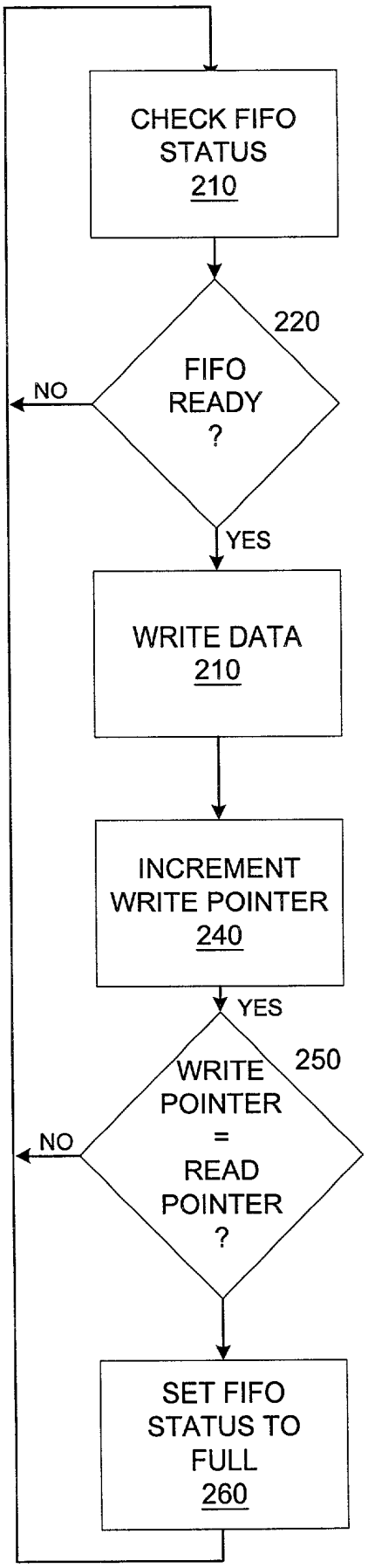
CHECK FIFO STATUS 210
220
FIFO READY ?
NO
YES
WRITE DATA 210
INCREMENT WRITE POINTER 240
YES
250
WRITE POINTER = READ POINTER ?
NO
SET FIFO STATUS TO FULL 260

FIG. 2

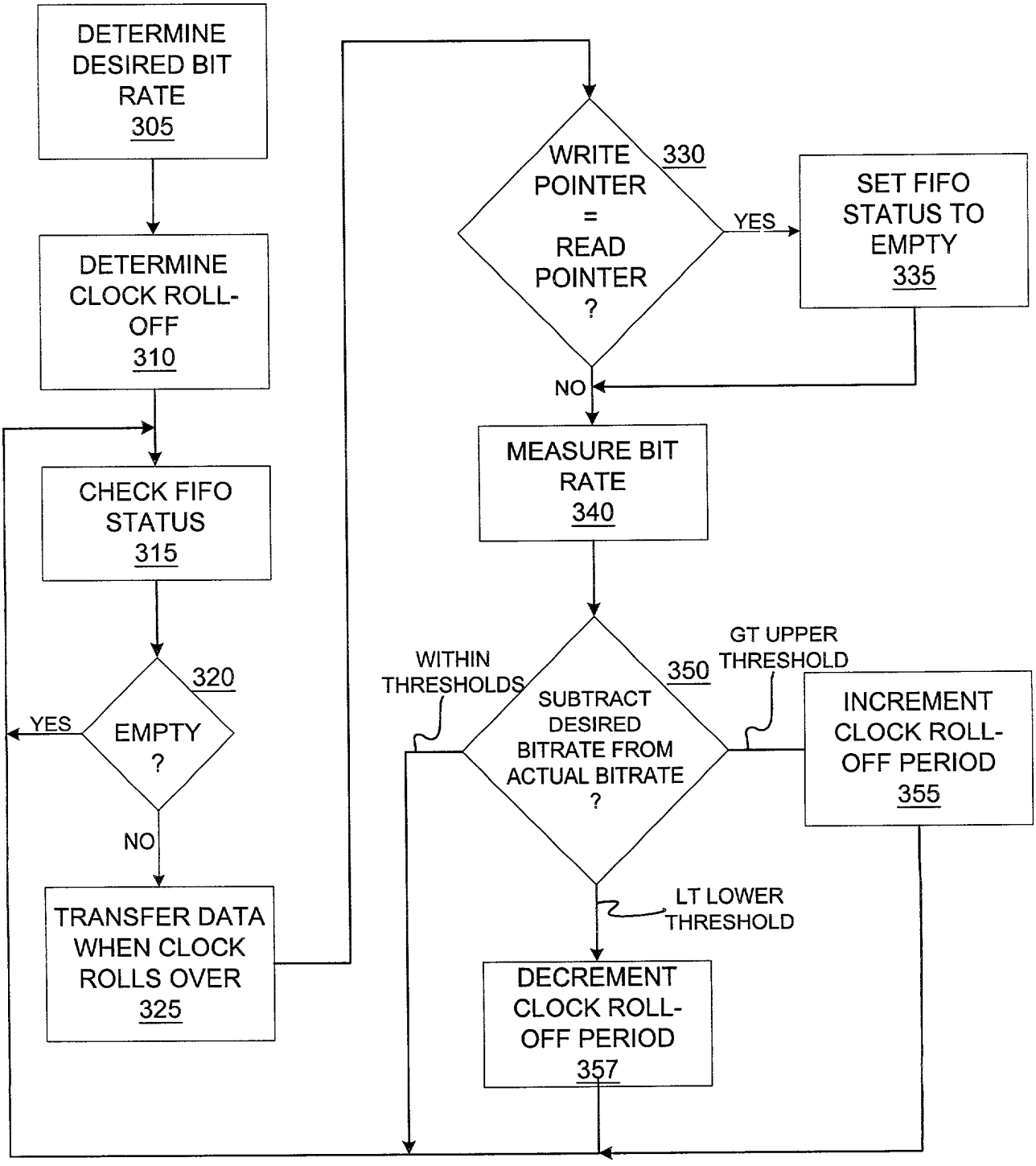
DETERMINE DESIRED BIT RATE 305
DETERMINE CLOCK ROLL-OFF 310
CHECK FIFO STATUS 315
320
EMPTY ?
YES
NO
TRANSFER DATA WHEN CLOCK ROLLS OVER 325
WRITE POINTER = READ POINTER ?
330
YES
SET FIFO STATUS TO EMPTY 335
NO
MEASURE BIT RATE 340
350
SUBTRACT DESIRED BITRATE FROM ACTUAL BITRATE ?
WITHIN THRESHOLDS
GT UPPER THRESHOLD
LT LOWER THRESHOLD
INCREMENT CLOCK ROLL-OFF PERIOD 355
DECREMENT CLOCK ROLL-OFF PERIOD 357

FIG. 3

TD_DATA_CNTL - RW -			
Field Name	Bits	Default	Description
TD_REG_DATA_MODE	0,1	'00'	0= normal operation, 1= register input mode. 2= bus mastered input mode. 3= reserved.
TD_DATA_RDY	2	'0'	Read only. Software has to check this field for next register write. Otherwise, data would be overwritten and corrupted.
TD_SYNC_LOST	12	'0'	read only . 0= normal operation, 1= data was overwritten.

TD_DATA - RW			
Field Name	Bits	Default	Description
TD_DATA	31:0	0x0	

TD_BM_MACRO_CNTL - RW			
Field Name	Bits	Default	Description
TD_BM_RST	0	0x0	0= no reset , 1= reset all pointers.
TD_BM_LOCK	1	0x0	0= normal operation, 1= lock the internal FIFO.
TD_BM_DEBUG	2	0x0	0= normal operation, 1= snoop into the FIFO (after locking).
TD_BM_LEAK_RATE	15:8	0x6	Control the data consumption from the BM FIFO read side. The value is in terms of MCLK cycles (GUI clock of 75MHz) between bytes.
TD_BM_ADDR	21:16	0x0	BM FIFO address, in lock and debug modes.

TD_BM_MACRO_DATA - RW			
Field Name	Bits	Default	Description
TD_BM_MACRO_DATA	31:0	0x0	

FIG. 4